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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,384	09/30/2003	Li-Jau Yang	CISCO-8091	9157

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SIERRA PATENT GROUP, LTD.
1663 Hwy 395, Suite 201
Minden, NV 89423

EXAMINER

PALIWAL, YOGESH

ART UNIT	PAPER NUMBER
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2135

MAIL DATE	DELIVERY MODE
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12/19/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/676,384

Applicant(s)

YANG ET AL.

Examiner

Yogesh Paliwal

Art Unit

2135

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/2/2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 3 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 4-12, 14-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

- Applicant's amendment filed on Oct 2, 2007 has been entered. Applicant has amended claims 1, 7, 8, 10, 17, 18, and 20. Currently claims 1-20 are pending in this application of which claims 3 and 13 are withdrawn from consideration.
- Examiner acknowledges amendment to claim 1 to recite data/control signals to overcome claim objection under 37 CFR 1.75(a). This amendment to claim 1 successfully overcome the claim objection, as a result, claim objection to claim 1 under 37 CFR 1.75(a) is withdrawn.
- Examiner acknowledges amendments to claims 7, 8, 10, 17, 18 and 20 that changed "serial wire interface" to "communication medium" to overcome claim objection under 37 CFR 1.75(d). These amendments to claims successfully overcome the claim objections, as a result, claim objection to claims 7-10 and 17-20 under 37 CFR 1.75(a) is withdrawn.
- Examiner acknowledges receiving the terminal disclaimer filed on 10/02/2007 to overcome provisional nonstatutory double patenting rejection. The terminal disclaimer has been recorded and has been approved. As a result, nonstatutory double patenting rejection of claim 1 is withdrawn.

Response to Arguments

1. Applicant's arguments, see pages 7-9, filed on Oct 10, 2007, with respect to the rejection(s) of claim(s) 1-2,4-12,14-20 under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon

further consideration, a new ground(s) of rejection is made in view of Dhir et al. (US 2005/0084076 A1).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 7, 8, 9, 10, 11, 15, 17, 18, 19 and 20 are rejected under 35

U.S.C. 102(e) as being anticipated by Dhir et al. (US 2005/0084076 A1), hereinafter

Dhir.

Regarding **Claim 1**, Dhir discloses an apparatus for providing link layer security in a Physical Layer Transceiver (PHY) comprising:

analog circuitry configured to transmit to, and receive data from, a data transmission medium (**Fig. 1, Numeral 106, and also at Paragraph 0028, "Signal line 106 provides a communication link between integrated circuit 100 and external data of a physical medium."**)

digital circuitry coupled to said analog circuitry (**Fig. 1, Numeral 108, MII**), said digital circuitry configured to transmit data/control signals to, and receive data/control signals (**Fig. 1, Control/data between MII and MAC**) from, a Media Access Controller (**Fig. 1, Numeral 110, MAC**)

a PHY communications module coupled to said analog and digital circuitry (**Fig. 1, Numerals 102 and 106, PHY-1 and PHY-2**);

a crypto engine coupled to said digital circuitry (**Fig. 1, Numeral 112 and Fig. 8, Numeral 321, "Encryption Engine"**, also refer to Paragraph 0029, "MAC component 110 is concerned with media access issues, such as whether token passing or contention will be used. It typically includes authentication and encryption functionalities... The data to and from the MAC is processed by processing component 112. For example, processing component 112 is used to implement higher layers of the reference model." and also refer to Paragraph 0051);

a crypto communications module coupled to said crypto engine (**See Fig. 6, Numeral 305, Encryption Algorithm(s) mod."**); and

said PHY communications module being operatively coupled to said crypto communications module (**Fig. 8, Numerals 301, 312, "Program Memory"**, also refer to Paragraph 004 "Program memory 312 stores programming instructions for configuring programmable gates 307, or more particularly configuration logic blocks 307.", Note: gates 307 contains encryption algorithms module see Fig. 6).

Regarding Claim 5, the rejection of claim 1 is incorporated and Dhir further discloses a master communications module coupled between said PHY communications module and said crypto communications module (**Fig. 1, Numeral 108, MII**)

Regarding Claim 7, the rejection of claim 1 is incorporated and Dhir further discloses that PHY communications module is configured to provide connectivity through a communication medium (**see Fig. 8, Numerals 301 and 312, WLAN transceiver is connected to program memory 312**)

Regarding Claim 8, the rejection of claim 7 is incorporated and Dhir further discloses that said communication medium is configured to communicate with a plurality of devices (**See Paragraphs 0044 and 45**)

Regarding Claim 9, the rejection of claim 8 is incorporated and Dhir further discloses that plurality of devices include at least one device that communicates at the PHY level (**Paragraph 0045, "baseband processor 324"**), and at least one device that performs both PHY and security functions (**Paragraph 0045, "encryption engine"**).

Regarding Claim 10, the rejection of claim 7 is incorporated and Dhir further discloses that said communication medium communicates with at least one device that performs both PHY and Security functions (**Paragraph 0045, "encryption engine 321"**).

Regarding **Claim 11**, Dhir discloses an apparatus for providing link layer security in a Physical Layer Transceiver (PHY) comprising:

analog circuitry means for providing connectivity to a data transmission medium **(Fig. 1, Numeral 106, and also at Paragraph 0028, "Signal line 106 provides a communication link between integrated circuit 100 and external data of a physical medium.")**

digital circuitry means coupled to said analog circuitry means **(Fig. 1, Numeral 108, MII)**, said digital circuitry configured to transmit data/control signals to, and receive data/control signals **(Fig. 1, Control/data between MII and MAC)** from, a Media Access Controller **(Fig. 1, Numeral 110, MAC)**

a PHY communications means coupled to said analog and digital circuitry means **(Fig. 1, Numerals 102 and 106, PHY-1 and PHY-2);**

a crypto engine means coupled to said digital circuitry means **(Fig. 1, Numeral 112 and Fig. 8, Numeral 321, "Encryption Engine", also refer to Paragraph 0029, "MAC component 110 is concerned with media access issues, such as whether token passing or contention will be used. It typically includes authentication and encryption functionalities... The data to and from the MAC is processed by processing component 112. For example, processing component 112 is used to implement higher layers of the reference model." and also refer to Paragraph 0051);**

a crypto communications means coupled to said crypto engine means **(See Fig. 6, Numeral 305, Encryption Algorithm(s) mod.)**; and

said PHY communications means being operatively coupled to said crypto communications module (**Fig. 8, Numerals 301, 312, "Program Memory", also refer to Paragraph 004 "Program memory 312 stores programming instructions for configuring programmable gates 307, or more particularly configuration logic blocks 307."**, Note: gates 307 contains encryption algorithms module see Fig. 6).

Regarding Claim 15, the rejection of claim 11 is incorporated and Dhir further discloses a master communications means coupled between said PHY communications means and said crypto communications means (**Fig. 1, Numeral 108, MII**)

Regarding Claim 17, the rejection of claim 11 is incorporated and Dhir further discloses that PHY communications means is configured to provide connectivity through a communication medium means (**see Fig. 8, Numerals 301 and 312, WLAN transceiver is connected to program memory 312**)

Regarding Claim 18, the rejection of claim 17 is incorporated and Dhir further discloses that said communication medium means is configured to communicate with a plurality of devices (**See Paragraphs 0044 and 45**)

Regarding Claim 19, the rejection of claim 18 is incorporated and Dhir further discloses that plurality of devices include at least one device that communicates at the PHY level (**Paragraph 0045, "baseband processor 324"**), and at least one device that performs both PHY and security functions (**Paragraph 0045, "encryption engine"**).

Regarding Claim 20, the rejection of claim 17 is incorporated and Dhir further discloses that said communication medium means communicates with at least one

device that performs both PHY and Security functions (**Paragraph 0045, “encryption engine 321”**).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 4, 6, 12, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhir in view of Lo (US 5,995,514), hereinafter Lo.

Regarding **Claims 2 and 12**, the rejection of claims 1 and 11 is incorporated and Dhir further discloses PHY communication module is configured to provide connectivity through an interface (**See Fig. 1, control signal from MAC to PHY-1 and PHY-2**) and said PHY controls the operation of said crypto device (**Fig. 8, Numerals 301 and 312 also paragraphs 0046, 0049**). Dhir does not explicitly disclose that these control signals are MDIO/MDC signals.

However using MDIO/MDC interface by media access controller is well-known. Lo discloses MDIO/MDC interface between MAC and PHY (**see Fig. 3, Column 2, lines 55-62**).

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize, in the communication integrated circuit of Dhir, MDIO/MDC interface as taught by Lo because *the MDC and MDIO signals are the signals for the serial management interface between the MAC device and PHY device (Lo, Column 2, lines 55-62)*. Also MDIO is well-known to provide user an option to change configuration information during operation, as well as read the PHY's status.

Regarding **Claims 4 and 14**, the rejection of claims 1 and 11 is incorporated and Dhir further discloses PHY communication module is configured to provide connectivity through an interface (**See Fig. 1, control signal from MAC to PHY-1 and PHY-2**); and said crypto communications module is coupled to said interface (**Fig. 1, MAC is connected with Processing 112 with control interface line and processing 112 is responsible for encryption and authentication, see paragraph 0029**). Dhir does not explicitly disclose that these control signals are MDIO/MDC signals.

However using MDIO/MDC interface by media access controller is well-known in the art of communication devices. Lo discloses MDIO/MDC interface between MAC and PHY (**see Fig. 3, Column 2, lines 55-62**).

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize, in the communication integrated circuit of Dhir, MDIO/MDC interface as taught by Lo *because the MDC and MDIO signals are the signals for the serial management interface between the MAC device and PHY device*

(Lo, Column 2, lines 55-62). Also MDIO is well-known to provide user an option to change configuration information during operation, as well as read the PHY's status.

Regarding Claims 6 and 16, the rejection of claims 1 and 11 is incorporated and Dhir further discloses that crypto communications module is configured to provide connectivity through a interface **(Fig. 1, MAC is connected with Processing 112 with control interface line and processing 112 is responsible for encryption and authentication, see paragraph 0029)**, and said crypto device controls the operation of said PHY **(See Fig. 1, data has to go through numeral 112 (processing) where it is encrypted and then passed onto either PHY-1 or PHY-2 for transmitting it to the external source through signal line 106. Since data has to be processed by encryption engine before it gets to either PHY-1 or PHY-2, this can be seen as encryption engine controlling the operation of PHY, by processing the data before it gets to the PHY)**. Dhir does not explicitly disclose that these control signals are MDIO/MDC signals.

However using MDIO/MDC interface by media access controller is well-known. Lo discloses MDIO/MDC interface between MAC and PHY **(see Fig. 3, Column 2, lines 55-62)**.

Therefore, it would have been obvious at the time the invention was made to one of ordinary skill in the art to utilize, in the communication integrated circuit of Dhir, MDIO/MDC interface as taught by Lo *because the MDC and MDIO signals are the signals for the serial management interface between the MAC device and PHY device*

(Lo, Column 2, lines 55-62). Also MDIO is well-known to provide user an option to change configuration information during operation, as well as read the PHY's status.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh Paliwal whose telephone number is (571) 270-1807. The examiner can normally be reached on M-F: 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

YP
12/10/2007


KIM VU
PATENT EXAMINER
EBC CENTER 2100